at least one interlayer insulating film formed over said electric current controlling element;

a contact hole opened in said interlayer insulating film;

a pixel electrode formed over said interlayer insulating film and electrically connected to said electric current controlling element through said contact hole;

an insulating layer comprising an organic resin formed on a portion of said pixel electrode in said contact hole;

a light emitting layer formed over said pixel electrode and said insulating layer; and

a second electrode formed over said light emitting layer.

16. (Twice Amended) The self-light-emitting device according to claim 15 wherein said electric current controlling element comprises a thin film transistor.

17. (Twice Amended) The self-light-emitting device according to claim 15 wherein said electric current controlling element comprises a transistor formed within a silicon substrate.

22. (Twice Amended) A self-light-emitting device comprising:

at least first and second electric current controlling elements;

at least one interlayer insulating film formed over said first and second electric current controlling elements;

at least first and second pixel electrodes formed over said interlayer insulating film wherein said first and second pixel electrodes are electrically connected to said first and second electric current controlling elements, respectively;

an insulating layer formed in a gap between said first and second pixel electrodes;

a light emitting layer formed over said first and second pixel electrodes and said insulating layer; and

a third electrode formed over said light emitting layer opposed to said first and second pixel electrodes.

23. (Twice Amended) The self-light-emitting device according to claim 22 wherein said electric current controlling element comprises a thin film transistor.

24. (Twice Amended) The self-light-emitting device according to claim 22 wherein said electric current controlling element comprises a transistor formed within a silicon substrate.

Cancel Claims 29, 32, 43, 46-50, and 58-63.

REMARKS

Applicants appreciate the Examiner's allowance of Claims 1-7, 35-42, 53-57, 65-68, 70-73, 75-78 and 80–83.

Applicants are submitting this amendment to place this application in a condition for allowance. Accordingly, it is requested that this amendment be entered.

Applicants will now address each of the Examiner's objections and rejections in the order in which they appear in the Final Rejection.